ALD Material Development at Argonne for LAPD Project

Godparent review meeting : 04/30/2011

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Outline

- Project background
- Achievements of ANL ALD Group
  - Delivered tasks in Year-2
  - Gain test setup
  - Publications
- ALD work updates
  - Gain test results
  - First Mocktile
- Plans for ALD Material Development at Argonne
  - 33mm MCPs requirements for (ALD lab, APS test, and UCB)
  - Improvement of existing optimized processes
- Plan for ALD on 8”x 8” MCPs and Grid spacers in BENEQ
  - Hardware modification
  - Time line
- Year 2 Milestones status
- Summary
- Acknowledgements

LAPD project background:

- To design and fabricate "economical, large area (8"x8") and robust" LAPDs with basic concept of MCP detectors with quantum efficiencies and gains similar to those of photomultipliers that used for wide range of applications.

- LAPD project divided into few sub-projects and ALD group at ANL is responsible for fully functionalization of various items with suitable kind of chemistry

Achievements of ANL ALD Group:

➔Delivered Items/Efforts in Year 2

Items	APS group	ALD Group	UCB group	Surface analysis Group	Comments
33mm MCPs	38	30	14		MCPs from old + new batch
8”x8” MCPs			3		Big triple point voids & a line cracked
Coupons			24	>25	SEE with and without Rs
Grid Space A		20			For Mocktile
Grid Spacer D		6			For Mocktile
George		6			For Mocktile
Mock tile MCPs	10				For Mocktile
Circular spacers		40			Plan dropped
Bad MCPs		~20			Big triple pints, bad depositions

Achievements of ANL ALD Group:

➔Publications

- Patent application = 1
- Poster presentation= 1 (SPIE 2011)
- Publication = 2
- Abstract submitted = 2
- Expected future ALD publications = 2-3
- ALD group co-authors in other LAPD publications = 2 (????)

Achievements of ANL ALD Group:

Design and construction of electrical measurement system for MCPs

Photograph of gain measurement setup:

EMWCD

Dual MCPs testing
(Possible to load 3 MCPs)

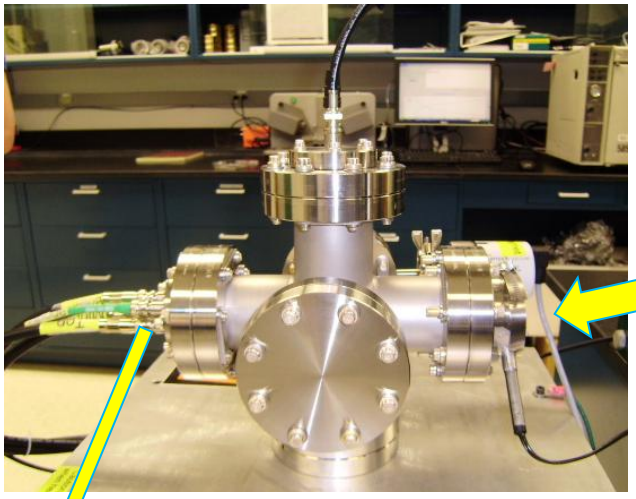
Labview Vi developed

pA current meter

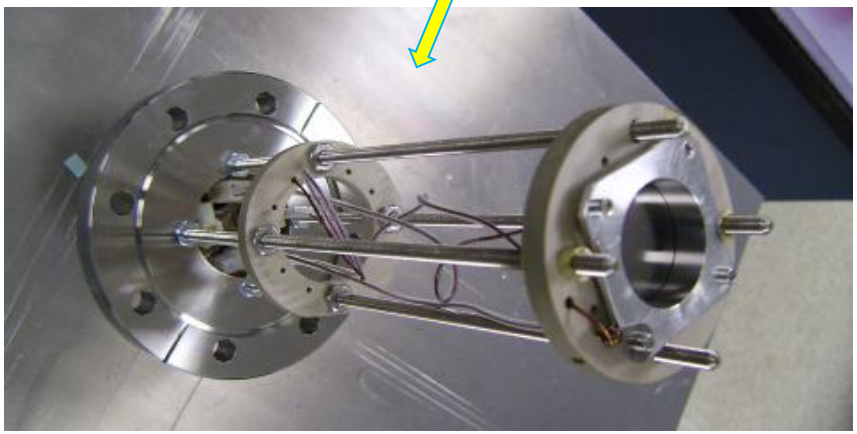
3 high voltage (0-5kV)
DC power supply

- Several MCPs electrical characteristic tested

HW design for MCP Gain test:



Shielded UV source for electron generation



MCP holder

Drain resistors box

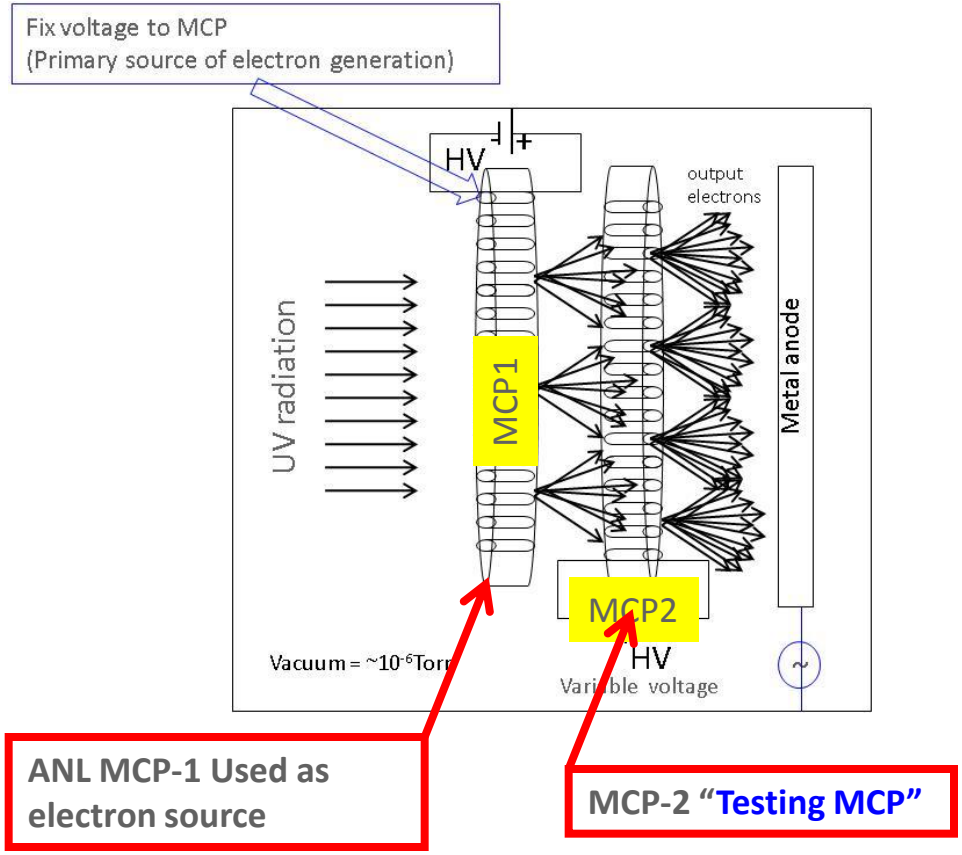
System capabilities:

- Current vs. Voltage (I-V)
- Resistance vs. Temperature (R-T) ➔ (Thermal coefficient , activation energy)
- Resistance vs. Time (R-t) @ fix HV
- Gain vs. voltage
- Long term stability under scrubbing condition
- Two optical windows (e.g. thermal imaging with CCD, phosphor screen)
- Easy to modify (Thinking about 2 more small chambers for life test?)

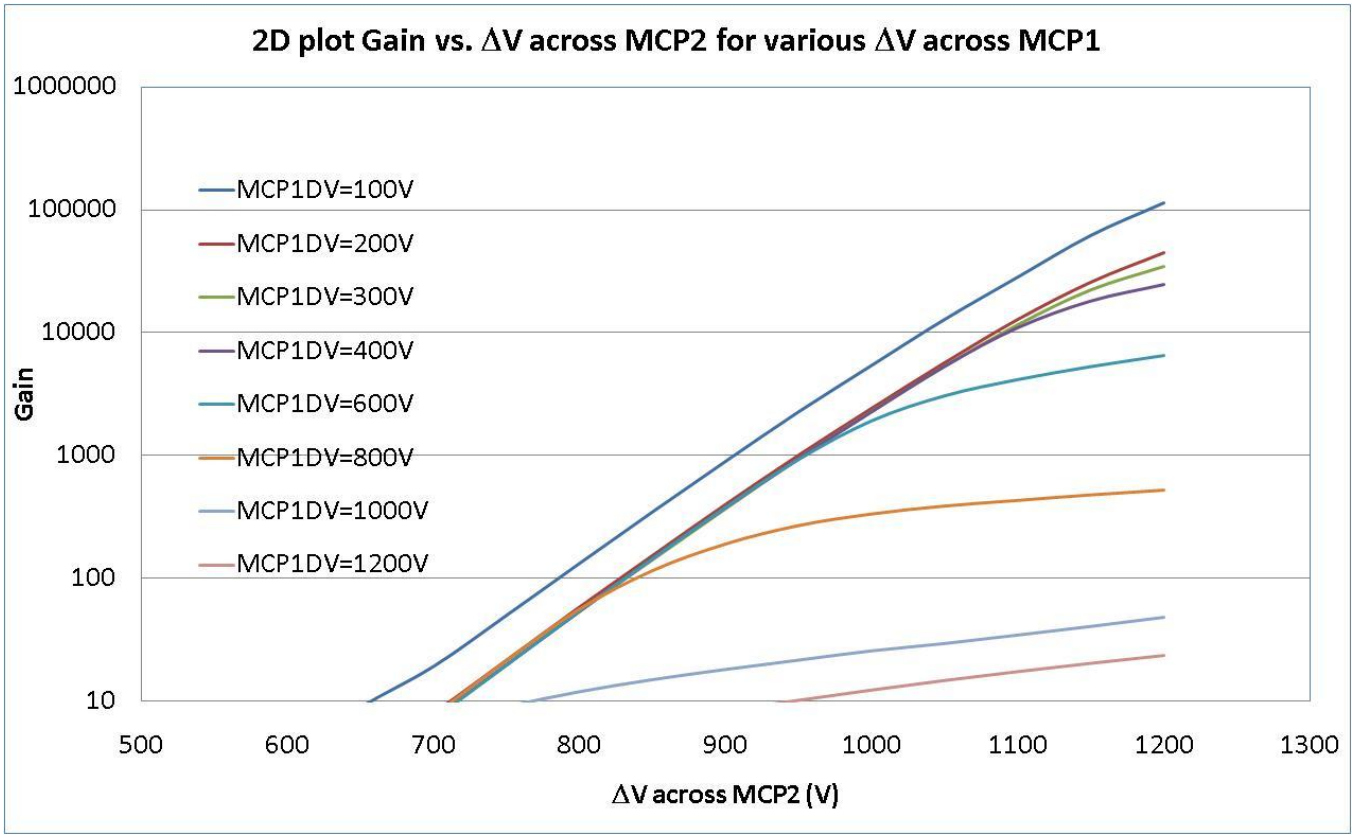
Objective:

Full electrical characterization of MCPs

Gain measurement arrangement :

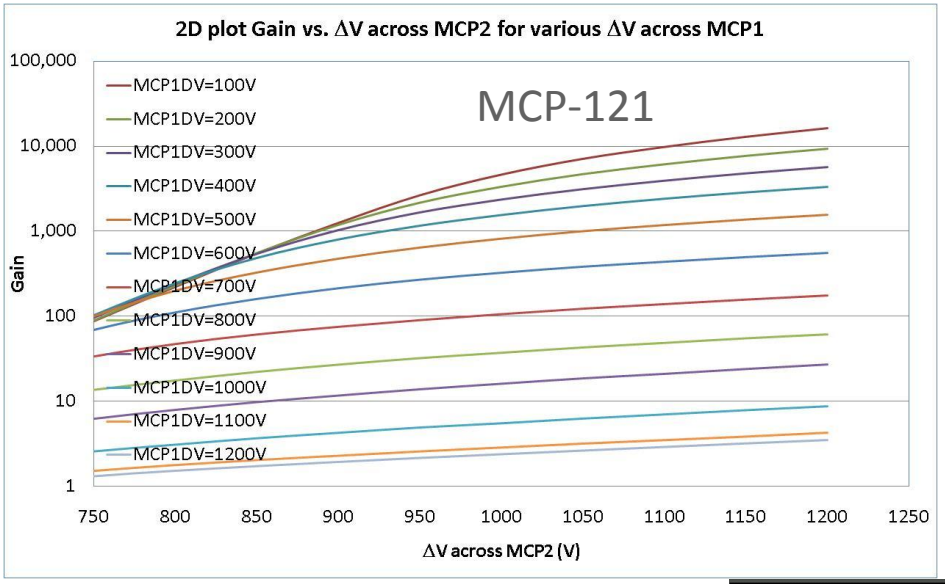


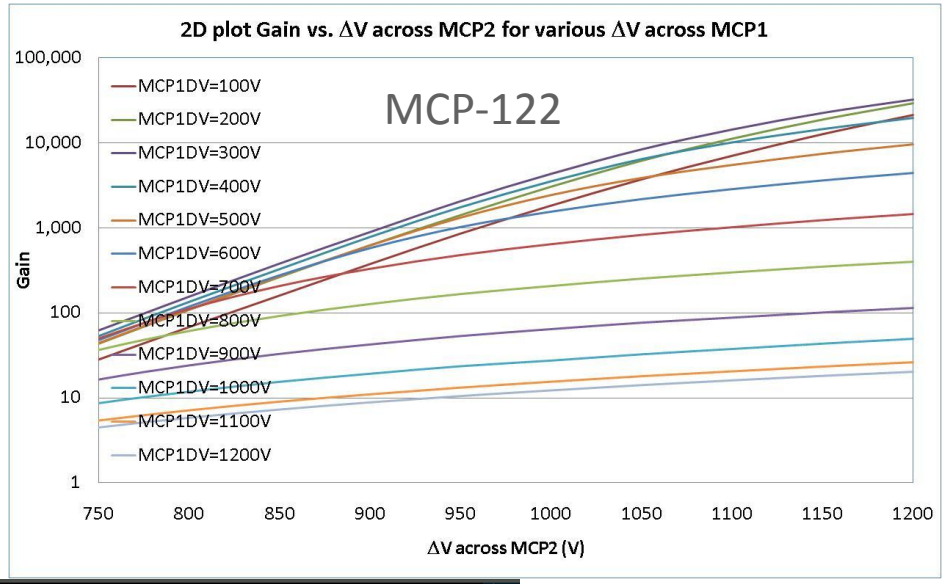
Gain data collection: e.g. MCP# 142

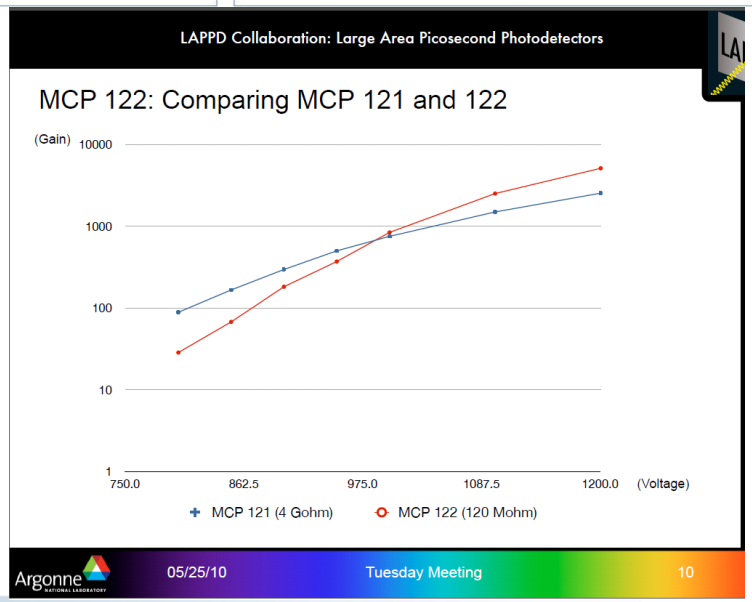


- 100k gain obtained

Gain data comparison: APS vs. ALD lab set-up







Courtesy Matt

MCP tests results:

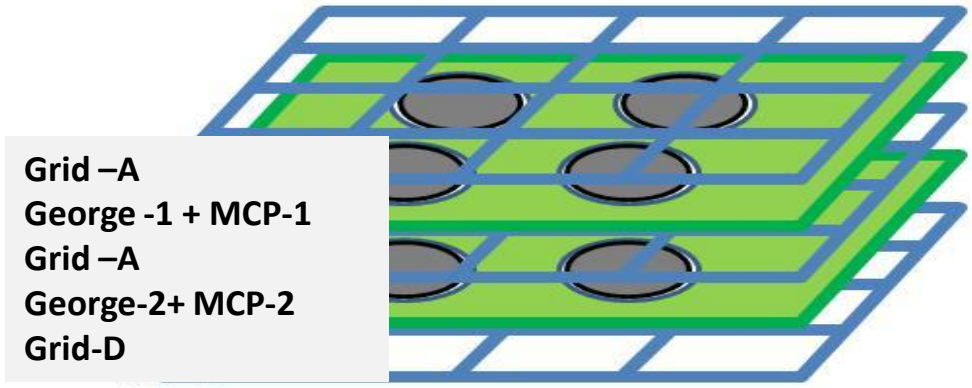
MCP ID	Rs Layer	SEE Layer	Resistance	Gain @ 1200V
1442(Photonis 40μm pore)	PbOx	PbOx	88MΩ	>100k
121 (300C)	Chem-1	ALO	4GΩ	16k also Tested at APS
122 (300C)	Chem-1	ALO	142MΩ	32k also Tested at APS
142	Chem-2	MgO	88MΩ	>100k
156	Chem-2	MgO	7MΩ(?)	>100k
114	Chem-2	ALO	58MΩ	>100k

MCP gain influenced by:

- **Input current**
- **Resistance of MCP**
- **Composition of Rs layer**
- **SEE layer**
- **Processing temperature**

Mock tile parts fabrication by ALD

Mocktile Schematic:



$R_{George} >>> R_{MCP}$

Note:

- Both current grid spacer A and D has sharp edges
- Grid spacer A is very fragile and has continuous chip off along the sharp edges
- Many broken pieces after packaging open

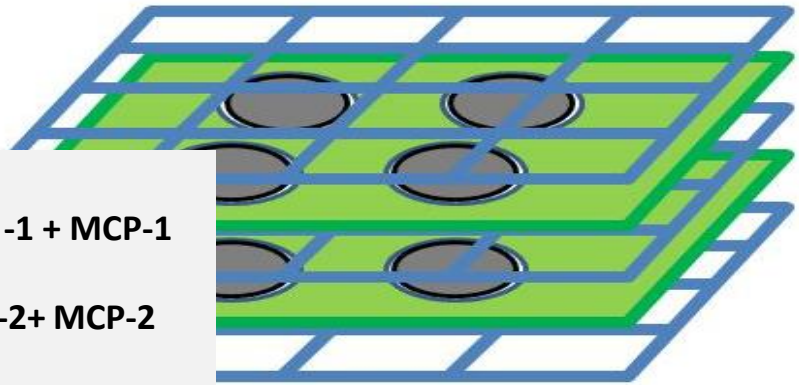
Requirements for Mock tile (Option # 1):

1) 4x pairs of 33mm MCPs
   - Process with ALD chemistry -2 + ALO SEE layer
   - Resistance of grid will be depend on the MCP resistance
2) Two Type “A (1.1mm)” 8”x8” grid spacers
3) One Type “D (3.1mm)” 8”x8” grid spacers
4) Two “George space” [glass pate with 4 x 33 mm holes]
   - 100x higher resistance than MCP

Mock tile parameters and fabrication:

Hypothesis:

1) Average R of MCP's = 115 MOhms
2) V across grid spacer A (After photocathode) = 300-800V acceptable range
3) E field for spacing = 200 V/mm
4) R George spacer=100* R of MCP1

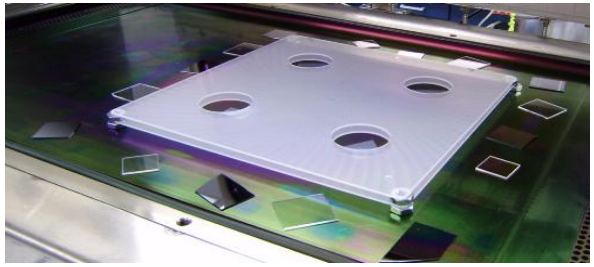


$R_{George} >>> R_{MCP}$

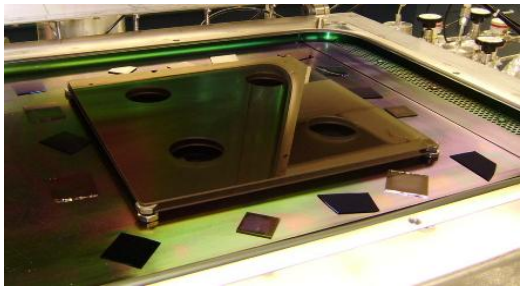
Layer	Thickness (mm)	# of items	R Item(MΩ)	R Layer(MΩ)	ΔV across item (V)	I(μA)
grid A	1.1	1		7.5	300	42
MCP-1	1.2	4	115	29.0	1200	42
grid A	1.1	1		7.5	300	42
MCP-2	1.2	4	115	29.0	1200	42
grid D	3.1	1		16.0	650	42
Total	7.7	11		89.0	3650	42
			RGeorge(Gohm)	10		

R of Grid spacer D ≅ 2* R of Grid spacer A

George spacers processing by ALD:



Before ALD

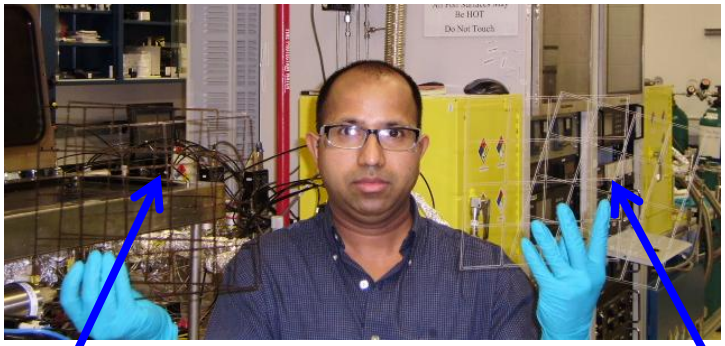


After ALD

Comparison

- **Processed 3 pairs of George Spacers**

Coating of Grid spacers by ALD:



Coated grid spacers as received grid

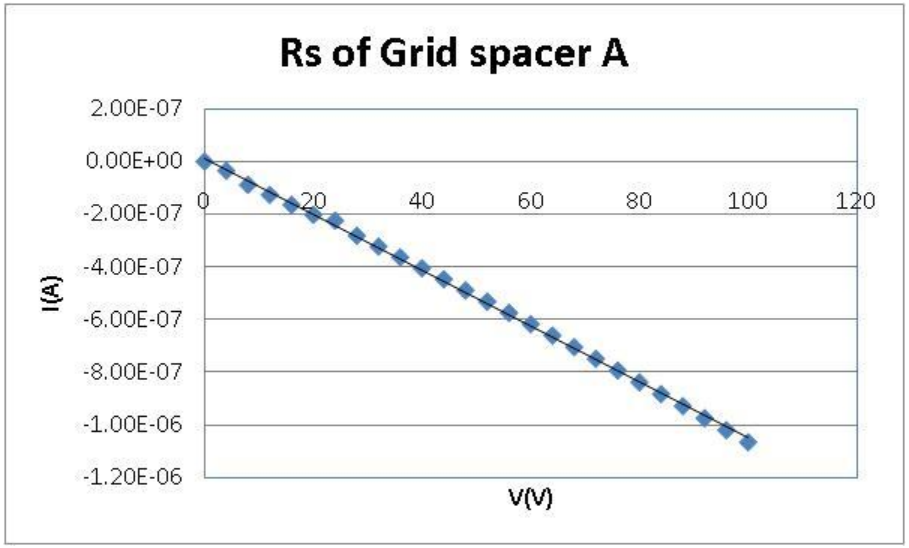
Grid spacer coated in batch (2-8 nos.)

Storage of ALD coated mocktile items:

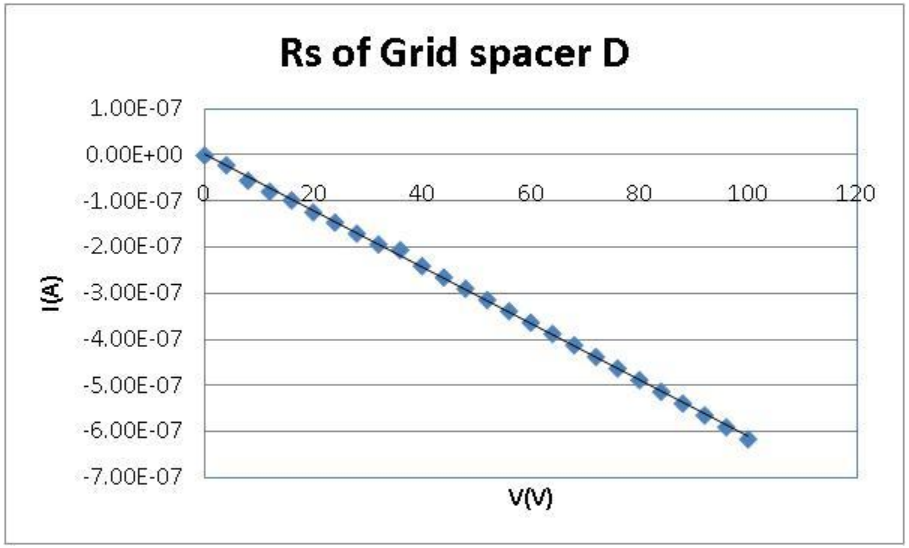
George spacer Type A grid spacer Type D grid spacer

Resistance of grid spacer A and D:

(Intermediate measurements)



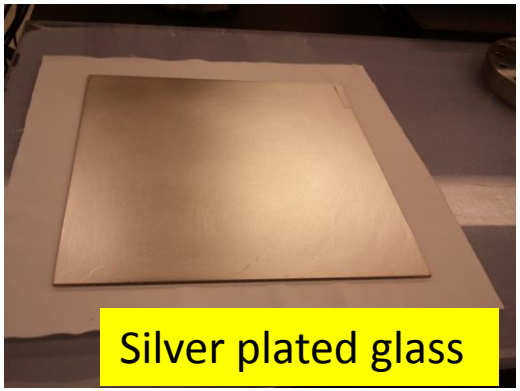
R=94MΩ

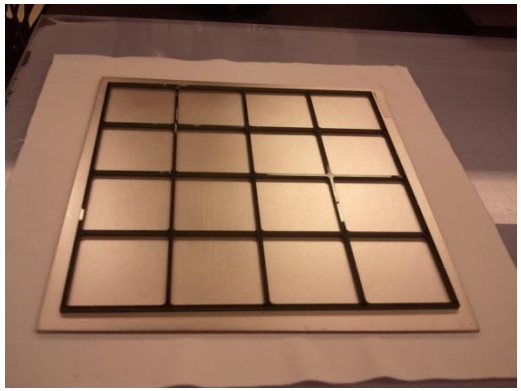


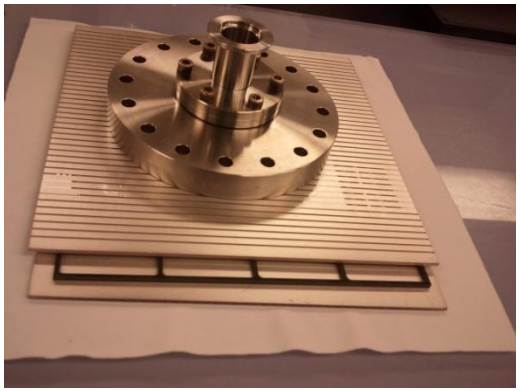
R=164MΩ

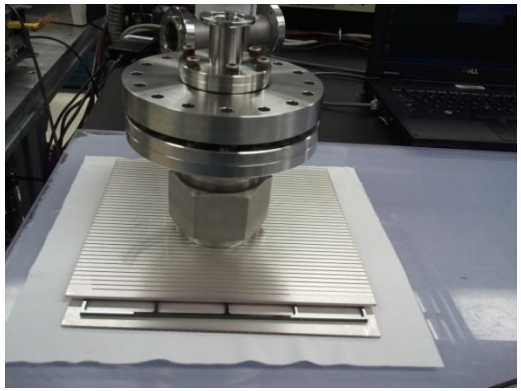
Rs of Grid spacer D ≅ 2* Rs of Grid spacer A

Resistance measurement:

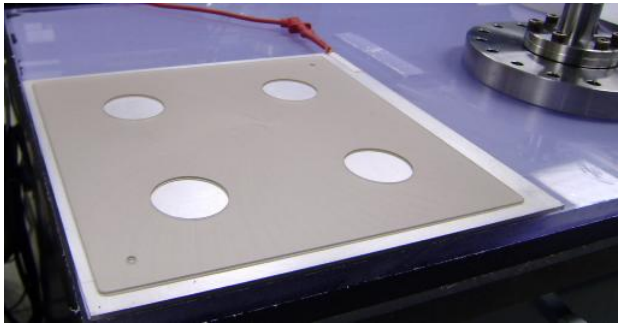






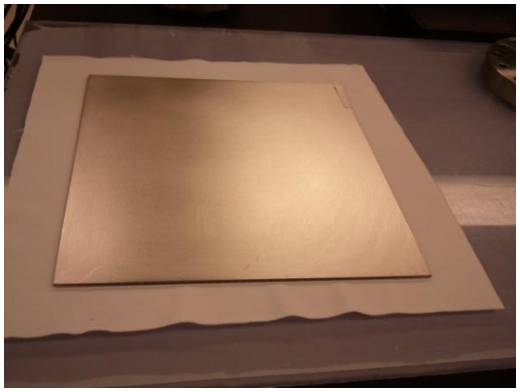


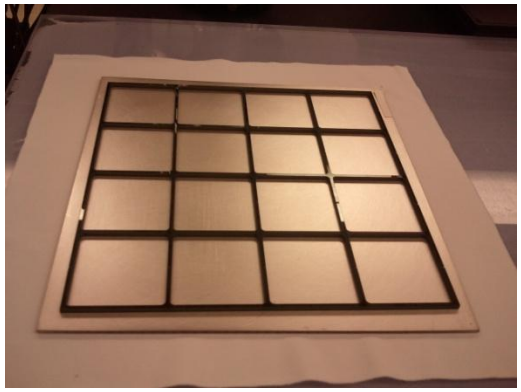
R is dependent on the load on electrode (contact)

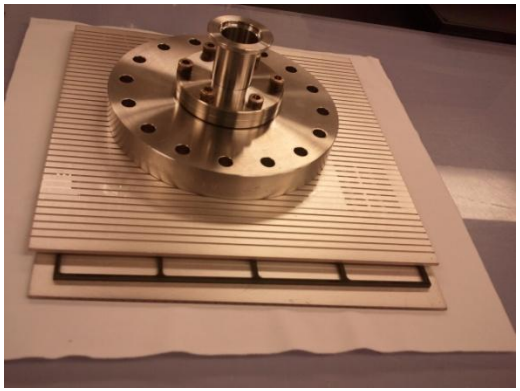


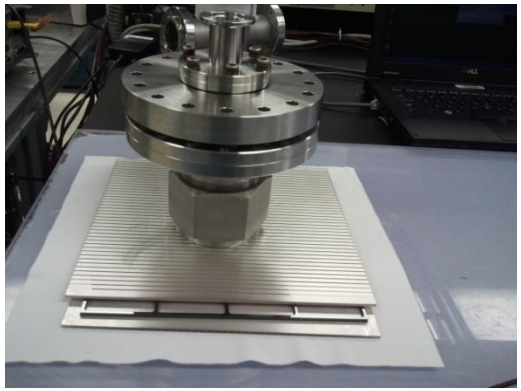
Resistance measurement:

Resistance of Grid Spacer (MΩ)	
Type-A	Type-D
0.13	--
0.13	--
--	0.4
--	0.4
530	--
400	--
10	16
17	--
38	--
64	--
380	700
135	1000
400	--
500	--
0.2	--
0.2	--
0.5	--
4	--
4	--
1	--
3	--
3	--
3	--
38	--
10	17
10	--
10	--
10	--
--	8
2	6
8	--
9	--

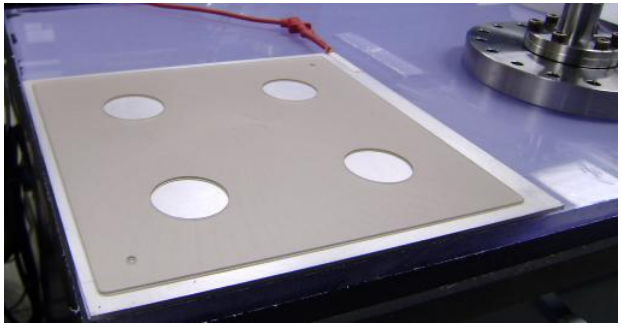






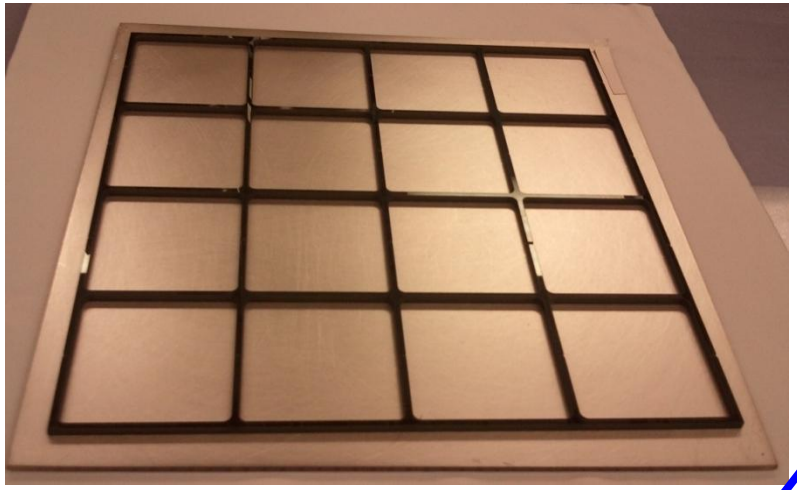


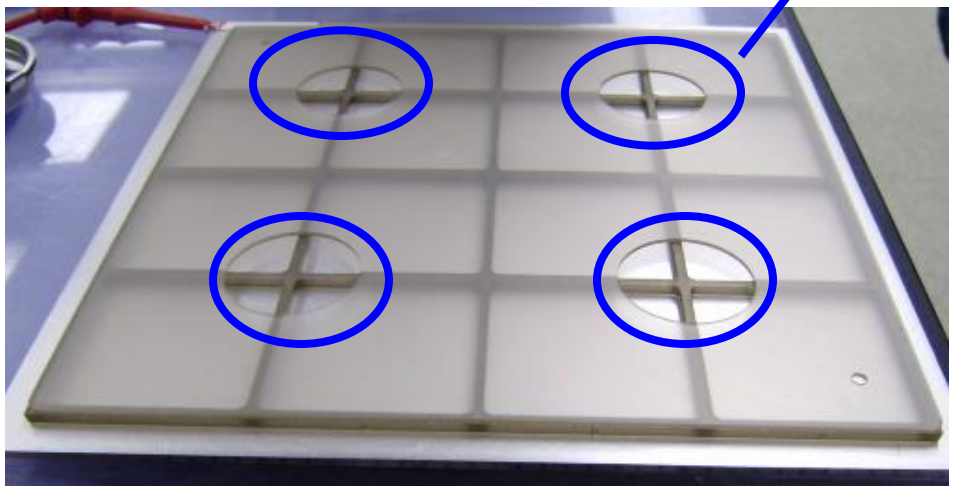
R is dependent on the load on electrode (contact)



Change in resistance due to geometry:

Resistance of Grid Spacer (MΩ)	
Type-A	Type-D
0.13	--
0.13	--
--	0.4
--	0.4
530	--
400	--
10	16
17	--
38	--
64	--
380	700
135	1000
400	--
500	--
0.2	--
0.2	--
0.5	--
4	--
4	--
1	--
3	--
3	--
3	--
38	--
10	17
10	--
10	--
10	--
--	8
2	6
8	--
9	--





$$R = \rho l / A$$

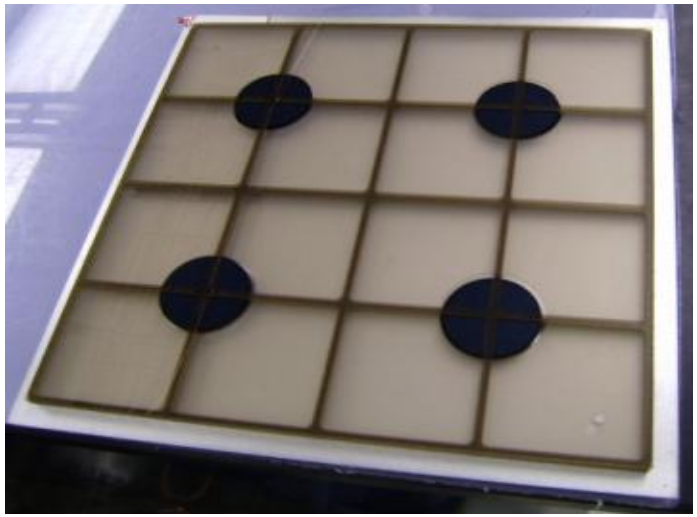
Mock tile components resistance:

Items	Individual component Rs (MΩ)	Actual Rs when stacked (MΩ)	Stack Rs after each component (MΩ)
Single MCP	115	NA	NA
Grid spacer D	1.66	13	13
Bottom 4xMCPs	29	28	41
Top 4xMCPs	29	27	75
Top grid spacer A	1.4	15	90
Total Rs =	61.52	90	85-100
Total Rs After sealing & evacuation =		????	

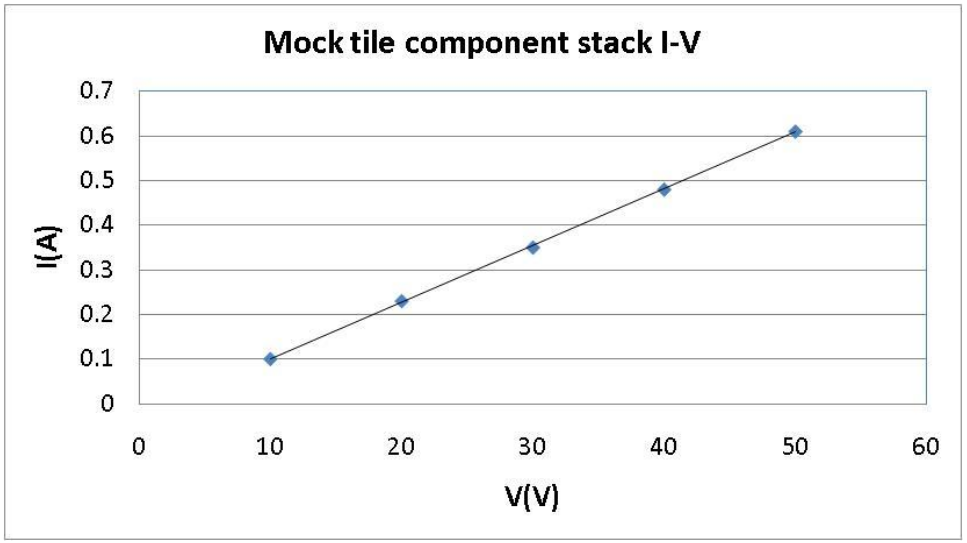
Closed to target value

Layer	Thickness (mm)	# of items	R Item(MΩ)	R Layer(MΩ)	ΔV across item (V)	I(μA)
grid A	1.1	1		7.5	300	42
MCP-1	1.2	4	115	29.0	1200	42
grid A	1.1	1		7.5	300	42
MCP-2	1.2	4	115	29.0	1200	42
grid D	3.1	1		16.0	650	42
Total	7.7	11		89.0	3650	42
			RGeorge(Gohm)	10		

Mock tile component stacked Resistance:

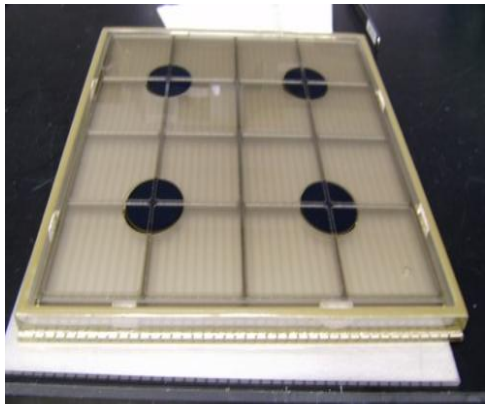


Before placing components into mocktile

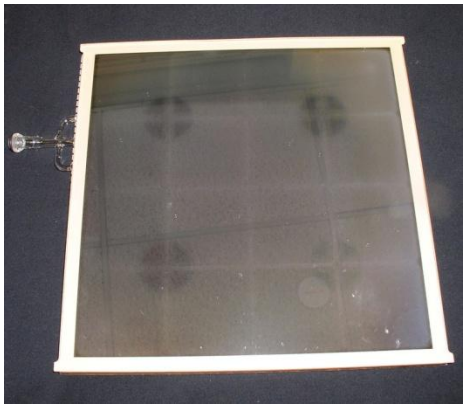


Stack of ALD processed components shows linear IV response (Resistance from IV before sealing = 84MΩ)

Construction of first mock tile:



a) Full stack ALD coated items in mock tile



b) Mock tile after sealing & evacuation

Courtesy: Joe & Dean

First mock tile prototype ready & waiting for APS test facility

Attention needed for mock tile:

- Electrical connections
- Current grid spacer A is very fragile?
- Grid space resistance
- Current/voltage distribution across the stack
  - -What potential we need to apply to mock tile (with only 2 contact)?
- Will Photocathode efficiency matters?
- Change of Photocathode properties during firing/sealing
- How hot MCPs will go during firing process?
- Will electrode on top or Bottom will matter during firing?

How do we improve?

- **Cleaning Procedure**
- **New grid spacer dimension = 2mm (better quality)**
- **NiCr Electrode on Grids (ASAP)**
- **Individual contact for each mocktile item**
- **High efficiency photocathode**
- **Back-up plan (few more mock tile and parallel approach)**
- **Start with 8”x8” MCPs sooner (simple integration scheme) ➔ MCP requirement**

➔**Requirements for Mock tile (Option#2):**
-2 Grid spacers + 1x (8”x8”) MCP

➔**Requirements for Mock tile (Option#3):**
-3 Grid spacers + 2x (8”x8”) MCP

For details Rich drawing on LAPD blog

MCPs requirements next ALD Development:

Items	APS group	ALD Group	UCB group	Surface analysis Group	Comments
33mm MCPs	20	30	12		In hand
8”x8” MCPs	12	15	12		New batch 10 MCPs arrived but 40 micron, New order placed
Coupons			??	??	SEE (with and without Rs)
Grid Spacer A		40			New vender
Grid Spacer D		20			New vender

- We have 20x 40micron 33mm MCPs
  - -Comparison purpose few MCP pairs testing will be OK?
  - -Time spending ?

Improvement of existing optimized ALD Processes:

- **The current optimized process “chem-2” is sensitive to ALD temperature**
  - **Amorphous vs. Crystalline?**
  - **Roughness effect (if any?)**
  - **Thin vs. Thick layer at low /high temperature processing conditions**

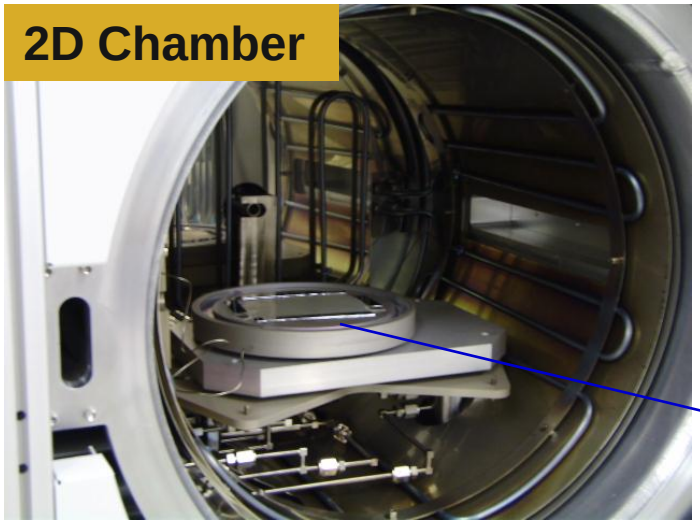
- **Introduce new SEE layers**
  - **MgF2 and CaF2**
  - **Amorphous vs. Crystalline?**

- **High temperature annealing (current 400C for 4 hrs)**
  - **RTA for few sec?**
  - **500C or 550C annealing for 1 hrs? (Incom glass MCPs survive)**
    - **Crystalline microstructure?**
    - **Gain /uniformity will improve? Or get worse?**

Plan for ALD on 8”x8” MCPs/Grid spacers:

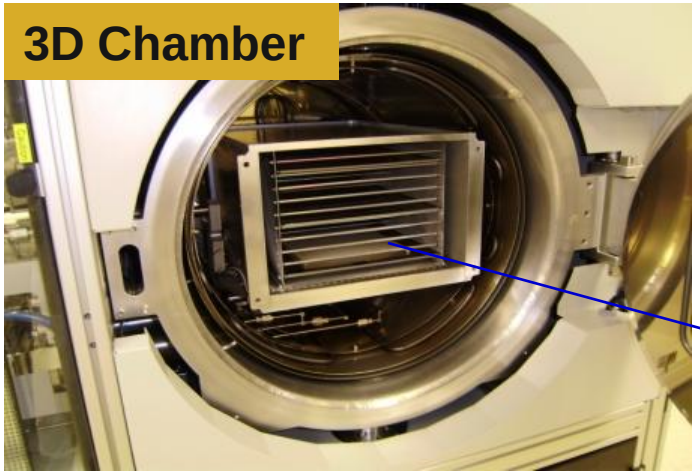
Beneq TFS 500 substrate loading configuration:

2D Chamber



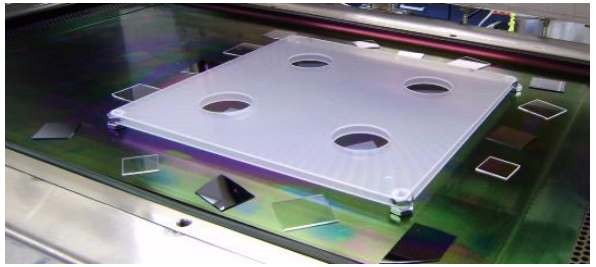
One 200mm wafer

3D Chamber



8”x8”MCP

ALD for 8”x8” MCPs:



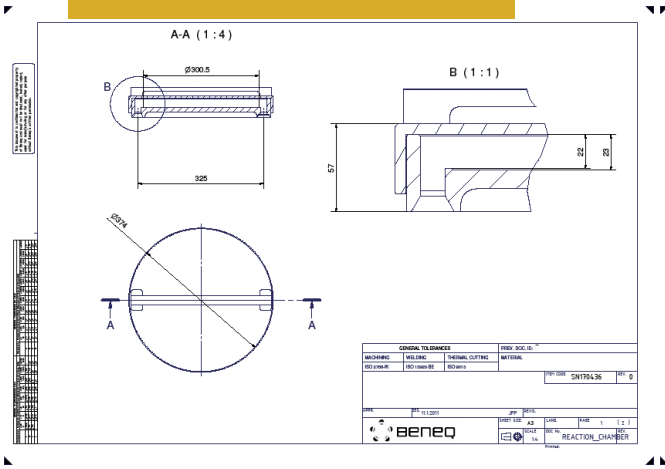
- Homebuilt (LSR) reactors and configuration time? Tool time?
- ALD in Beneq 3D chamber
  - Different process parameters for 2D (single 200mm wafer) Vs. 3D chamber (multi substrates)
  - Current 2D chamber can not accommodate a 8”x8” MCP square geometry
  - 3D chamber has very large volume
    - Good for batch production but not for 1-2 MCPs
    - Wastage of precursor
    - Time

ALD for 8”x8” MCPs:

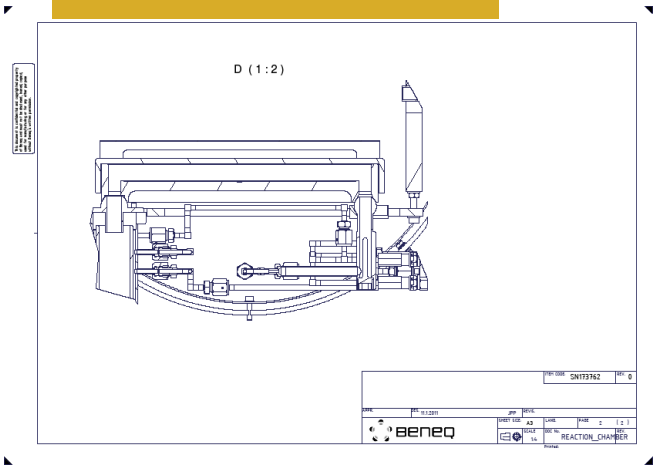
- Homebuilt (LSR) reactors and configuration time?
- ALD in Beneq 3D chamber
  - Different process parameters for 2D (single 200mm wafer) Vs. 3D chamber (multi substrates)
  - Current 2D chamber can not accommodate a 8”x8” MCP
  - 3D chamber has large volume
    - Good for batch production but not for 1-2 MCPs
    - Wastage of precursor
    - Time
  - Designed and asked Beneq to build a new custom made 2D chamber
    - Placed order in Jan 2011 and chamber delivery = May first week (Process testing going on)
    - Possible to process 2-4 (8”x8” MCPs)
    - Less precursor and good for 33mm and 8”x8” MCPs development work

New Beneq 2D chamber for 8”x8” MCPs:

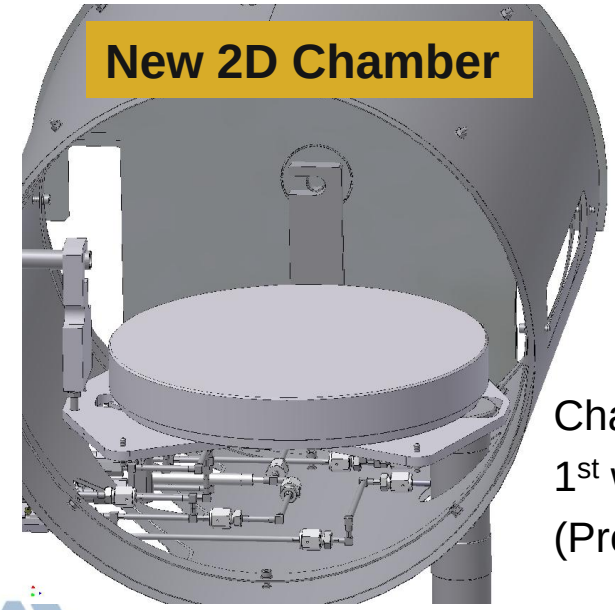
New 2D Chamber



New 2D Chamber



New 2D Chamber



Chamber will deliver in
1st week May
(Process testing going on)

Current 2D Chamber

ALD for 8”x8” MCPs:

- Homebuilt (LSR) reactors and configuration time?
- ALD in Beneq 3D chamber
  - Different process parameters for 2D (single 200mm wafer) Vs. 3D chamber (multi substrates)
  - Current 2D chamber can not accommodate a 8”x8” MCP
  - 3D chamber has large volume
    - Good for batch production but not for 1-2 MCPs
    - Wastage of precursor
    - Time
  - Designed and asked Beneq to built new custom made 2D
    - Possible to process 2-4 (8”x8” MCPs)
    - Placed order in Jan 2011 and chamber delivery = May first week (Process testing going on)
    - Less precursor and good for 8”x8” MCPs development work
  - Other facilities are ready
    - Flammable Gas cabinet with water line
    - Dose valves testing with dummy gases
    - Water scrubber for exhaust

Time line: ALD on 8”x8” MCPs and Grid spacers:

Nos.	Items	May 11	June 11	July 11	Aug 11
1	New 2D chamber HW testing	x			
2	Rs process testing and optimization on 33mm MCPs	x	x		
3	Batch processing test for 33mm MCPs (uniformity Thickens & Rs)		x		
4	Process testing on 8”x8” MCP		x	x	
5	Batch (2-4 MCPs) processing			x	x
6	Grid Spacer depositions	x	x		

Year 2 Milestones for ALD Group:

No.	Milestones	Comments
a	Demonstrate gain > 1000, non-uniformity to < 15%	Done
b	Optimize process economics for batch production	Next slide
c	Develop multi-dynode stripe coating of channel SEE layers for narrowing gain and transit-time spreads;	Feasible plan

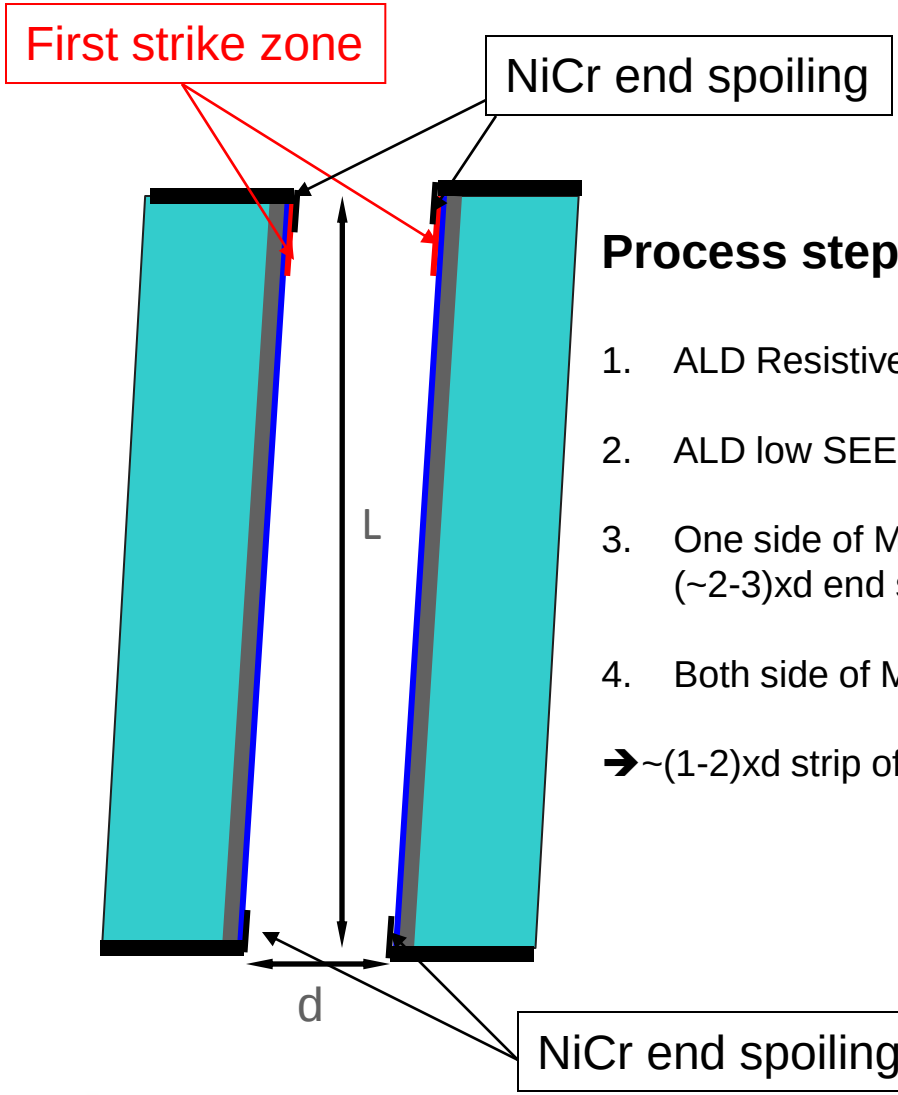
ALD optimize process economics for batch production:

- **Calculation for 200x 33mm MCPs with Resistive +SEE layers = 1000A**

Items	Cost $
ALD Precursors	5500
Gases	500
Substrates Si, Quartz	500
Pump oil	500
Other	1000
Total cost /MCP	40$

- **Calculation for 8”x8” MCPs will based on optimized process (TBD)**

Realistic propose plan to develop multi-dynode stripe coating of channel SEE:



Process steps:

1. ALD Resistive
2. ALD low SEE (e.g Al2O3)
3. One side of MCP PVD (evaporation) of High SEE with desire angle (~2-3)xd end spoiling (E.g. MgO)
4. Both side of MCP PVD (evaporation) NiCr (~1xd)

➔~(1-2)xd strip of high SEE coating“first strike zone” for narrowing gain

Summary

- Delivered items in year 2
- First mocktile fabrication
- Gain test setup and testing results
- MCP requirements for ALD development and testing group
- Large are MCP grid deposition plan and timeline
- Year 2 milestones
  - Optimized ALD process cost for 33mm MCPs
  - Realistic Strip coating plan

•Acknowledgement:

-Fermi lab (Eileen) for Electrode deposition

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- Prof. Henry and Bob for constant support

Thank you !!